REMARKS/ARGUMENTS

In accordance with the Examiners request the title of the specification has been changed.

The Examiner also objected to the specification for failing to provide proper antecedent basis for the claimed subject matter. The specification has been amended in order to overcome this objection by more clearly referencing terms in the claims to structures already described in the specification and the drawings. No new matter has been added by this amendment

The Examiner rejected Claim 29 under 35 U.S.C. 112 as being indefinite. Applicant believes that by the amendment of the specification this rejection is now overcome in that the features referred to in the claim are now more clearly described in the specification.

Claims 21 to 34 were rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,097,161 (Takano et al.) in view of US Patent No. 5,006,974 (Kazerounian et al.). The applicant has reviewed both the Takano and Kazerounian references and believes that they neither disclose nor suggest the invention as defined in the claims, either taken singly or in combination. Accordingly, the Examiner is requested to reconsider the rejection in view of the discussion below.

In general terms the present invention teaches a cascaded charge pump power supply, wherein the overall size of the charge pump is reduced by taking advantage of the high transconductance and gate capacitances per unit area of thin oxide devices while obtaining similar performance as the larger thick oxide devices in the subsequent stages of the cascade. Thus the present invention

provides a charge pump circuit having different gate oxide thickness transistors, as defined in independent claims 21 and 30.

In formulating this argument, the Examiner has stated that while Takano does not explicitly disclose the second oxide thickness of the FETs in the last pump stages, the teachings of the Kazerounian reference would motivate one skilled in the art to modify Takano to use pump stages of differing oxide thicknesses to ensure that the Takano charge pump circuit does not breakdown on operating in a high voltage environment. Applicant submits with due respect that this conclusion is only possible in hindsight of the applicants specifications. Not only do the references not suggest the invention, but they also do not provide any no motivation to a person skilled in the art to combine them..

Firstly, in Takano, the primary reference, there is no suggestion of its charge pump circuit breaking down when operating in high voltage environment. Consequently there is no motivation for a person skilled in the art to consider the Takano teaching when faced with this problem. One of Takano's objectives is to realise a low power consumption booster circuit.

Secondly, Takano does not teach nor suggest the use of transistors having differing oxide thicknesses. Further supporting the position that Takano did not consider the problem of space saving or voltage breakdown

Thirdly, although Takano has two cascades, they are powered by two separate sets of clock signals (see figure 4). In the present invention there is described only two such clocks which drive the two cascades.

Clearly, for all the above reasons Takano is not a valid primary reference.

On the other hand, Kazerounian relates to a circuit for EEPROMs not DRAM's as in the present invention. Kazerounian teaches using floating gate FETs in the charge pump. In fact each charge pump stage has floating gate FET configured as a diode and capacitors are explicitly described as parallel plate types. Kazerounian teaches the process for building the proposed devices, as shown in Figure 9, wherein layer 436 is the gate oxide deposition layer and is the same for both normal FETs and floating gate transistors. The floating gates receive a second oxide which forms the floating gate to control gate oxide. It is clear from Kazerounian that the same oxide thickness is used between the substrate and the floating gate as between the substrate and a regular gate. Therefore Kazerounian teaches the use of the same gate oxide thickness for all transistors.

Accordingly, assuming that the Examiner is correct in his argument that Takano misses the fundamental feature of differing gate oxide thicknesses, in order for the Examiner to make a valid obviousness type rejection Kazerounian would have to teach at a minimum the use of differing gate oxide thicknesses. Clearly, this aspect is missing not only from Kazerounian but also for Takano. For this reason Takano and Kazerounian cannot be combined to forma valid obviousness type rejection.

Furthermore, Kazerounian uses a floating gate structure as its essential enabler for the invention. It is well known in the art that a floating gate is not used in a DRAM and therefore the teachings of Kazerounian cannot be applied to a DRAM process. In fact, it would not be obvious or technically correct to adopt such EEPROM specific techniques in a DRAM charge pump. Accordingly, for this further reason Kazerounian is an invalid combination with Takano in formulating an obviousness type rejection.

Finally, with respect to the prior art US Patent No. 6,473,321 (Kishimoto) which the Examiner considers pertinent to the Applicant's disclosure, Applicant wishes to note that Kishimoto teaches that the different oxides are formed by the process steps so the EEPROM specific oxide is added to the base gate oxide. These different oxide thicknesses require manipulating the existing process sequence of an EEPROM process which once again is specific to EEPROMs. Applicant would further argue that it would not be obvious to a person skilled in the art to take an EEPROM specific process and apply it to the DRAM charge pump as described in the Applicant's disclosure.

For the above reasons the rejection of independent claims 21 and 30 is overcome.

With respect to the Examiner's rejection of Claims 22 to 29 and 31 to 43 these claims are dependent on what is believed to be a patentable base claims 21 and 30 respectively. Accordingly, the rejection of Claims 22 to 29 and 31 to 34 is also overcome.

Applicant also submits herewith for consideration a method Claim 35 which is based on Claim 21. It is believed for the reasons stated above that this new claim is also patentable and does not necessitate a new search.

Finally applicant submits under separate cover, and on concurrent date herewith an Information Disclosure Statement listing a reference which has come to the applicant's attention.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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